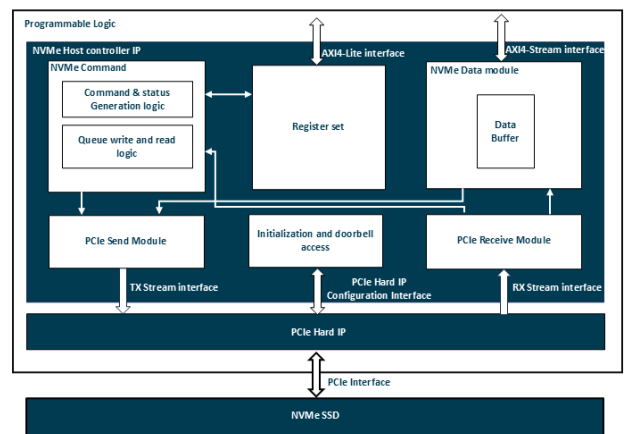


NVMe Host Controller IP Core

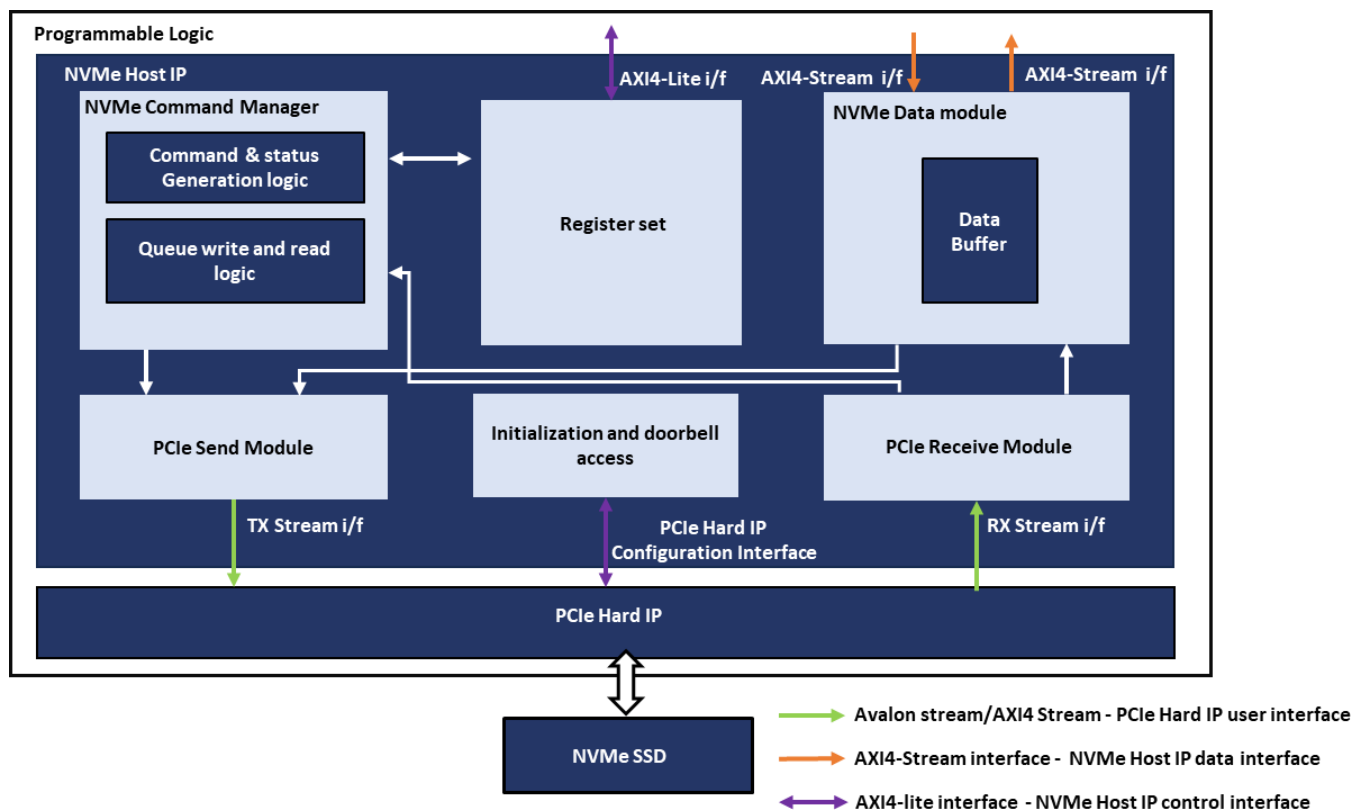
iWave's NVMe Host Controller IP Core is compliant with the NVM Express base specification revision 1.4, enabling seamless memory transfers to and from NVMe storage devices. iWave's NVMe Host Controller IP Core uses internal memory as data buffer, external DDR is used in the data path for the applications that does not accept any data backpressure. IP Core interfaces via PCIe, making it ideal for high-performance, large-capacity storage applications. The core features an AXI4-Lite interface for control and status register access and an AXI-Stream interface for data transfer.



Highlights

- ❖ Includes on chip buffer for data buffering
- ❖ Supports sustained writes using DDR buffering in the data path
- ❖ Supports debug & performance monitoring registers.
- ❖ The iWave NVMe IP core is tested with multiple SSDs from multiple vendors with different controllers ensuring compatibility and robust performance across a diverse range of storage solutions.

Block Diagram



Technical Specifications

NVMe Host Controller

- Compliant with NVM Express base specification revision 1.4
- Admin Command Supported:
 1. SMART/Health information
 2. Identify Controller data Structure
 3. Identify Namespace data structure
 4. Secure Erase
 5. Shutdown command
 for efficient NVMe device management.
- NVM Command Supported:
 1. Write Command
 2. Read Command
 3. Flush command
 for reliable and high-performance data transfer.
- Operates with LBA size of 512 Bytes
- Operates with Vendor specific PCIe Hard IP as a physical layer to access NVMe SSD
- User data interface: AXI4 – Stream
- User control interface: AXI4- Lite

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Since 1999, we have pioneered leadership in embedded systems technology, establishing ourselves as a strategic embedded technology partner for advanced solutions. Our comprehensive portfolio encompasses ARM and FPGA System on Modules, COTS FPGA solutions, and ODM solutions which include Telematics, Gateways & HMI Solutions.

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